FIG.1

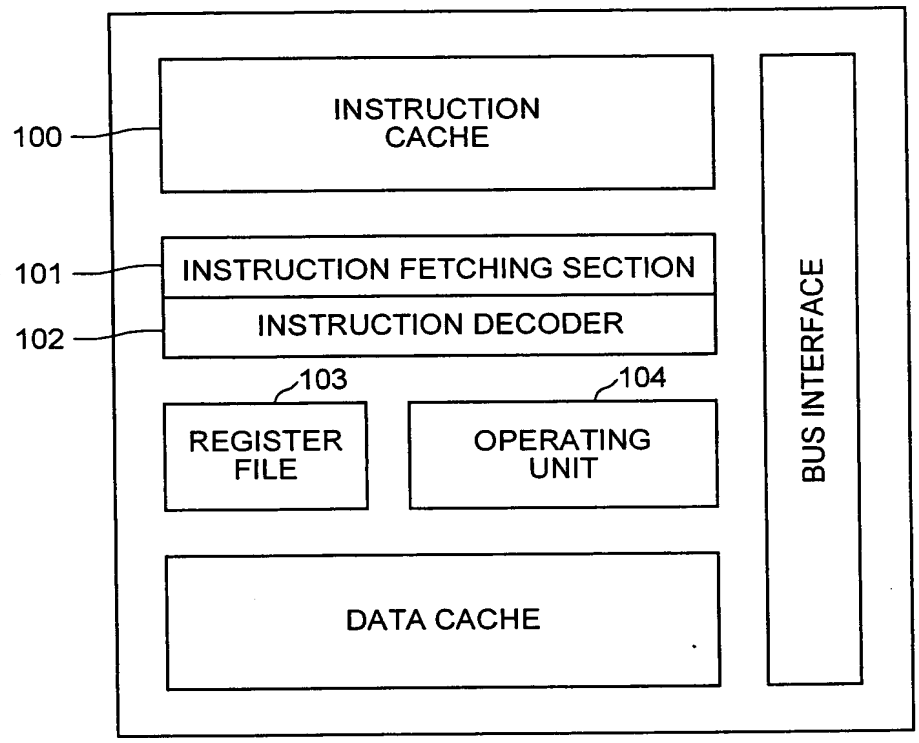

100
INSTRUCTION CACHE
101
INSTRUCTION FETCHING SECTION
102
INSTRUCTION DECODER
103
104
REGISTER FILE
OPERATING UNIT
DATA CACHE
BUS INTERFACE

FIG.2

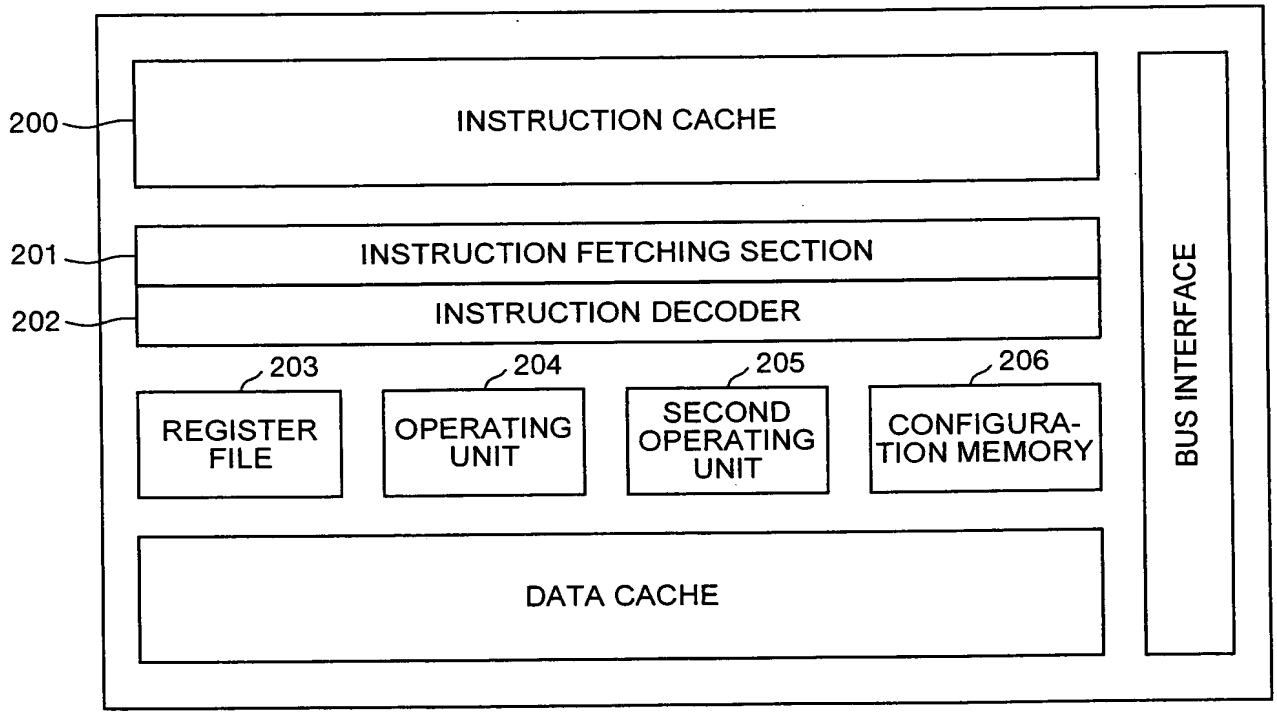

200
INSTRUCTION CACHE
201
INSTRUCTION FETCHING SECTION
202
INSTRUCTION DECODER
203
204
205
206
REGISTER FILE
OPERATING UNIT
SECOND OPERATING UNIT
CONFIGURA-TION MEMORY
DATA CACHE
BUS INTERFACE

FIG.3

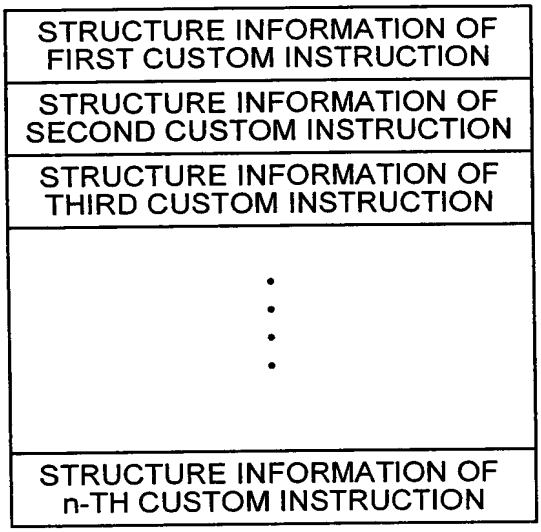
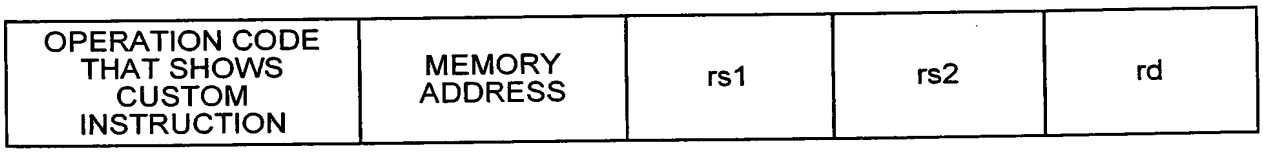


FIG.4



rs1:SOURCE REGISTER 1
rs2:SOURCE REGISTER 2
rd:DESTINATION REGISTER

FIG.5

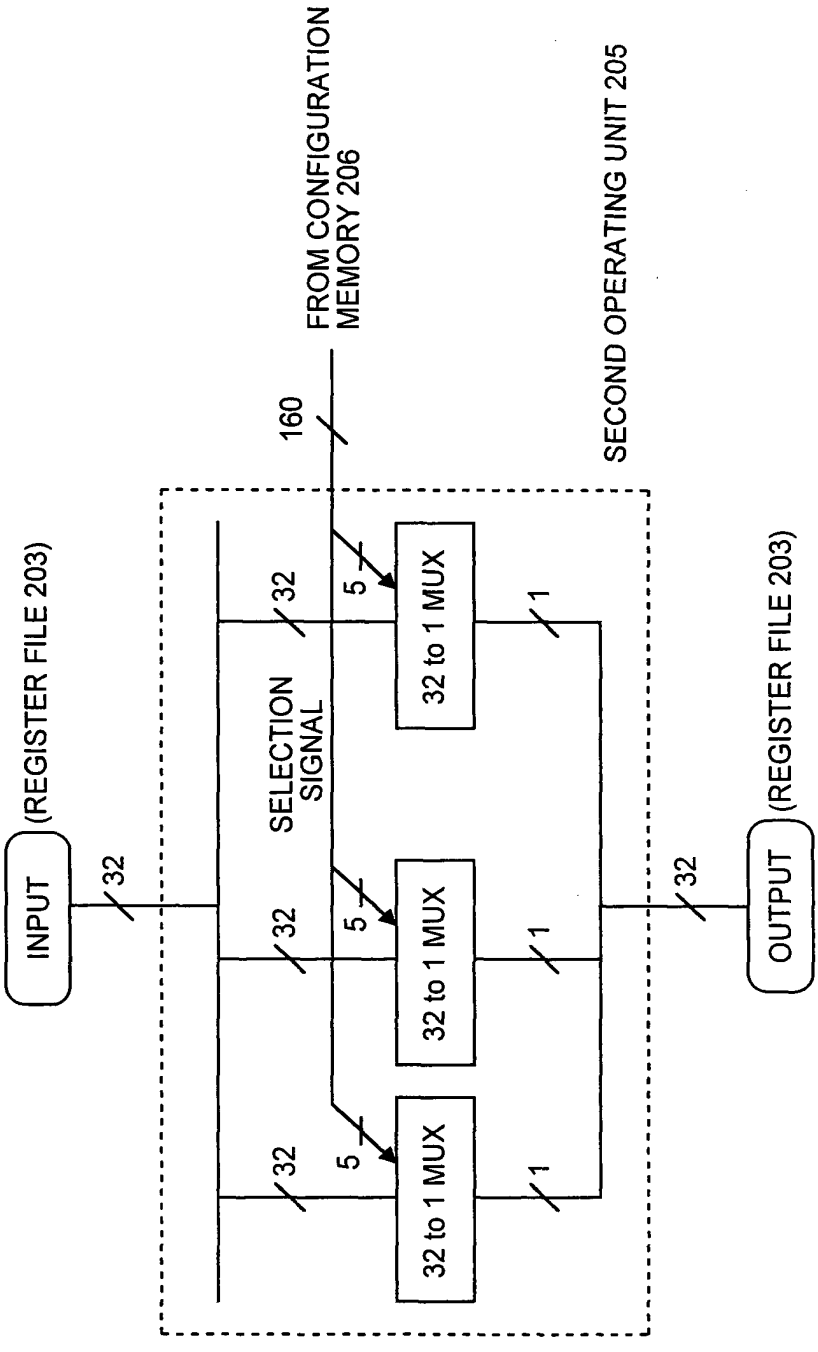

INPUT
(REGISTER FILE 203)
32
SELECTION SIGNAL
32
5
32 to 1 MUX
1
160
FROM CONFIGURATION MEMORY 206
SECOND OPERATING UNIT 205
OUTPUT
(REGISTER FILE 203)

FIG.6

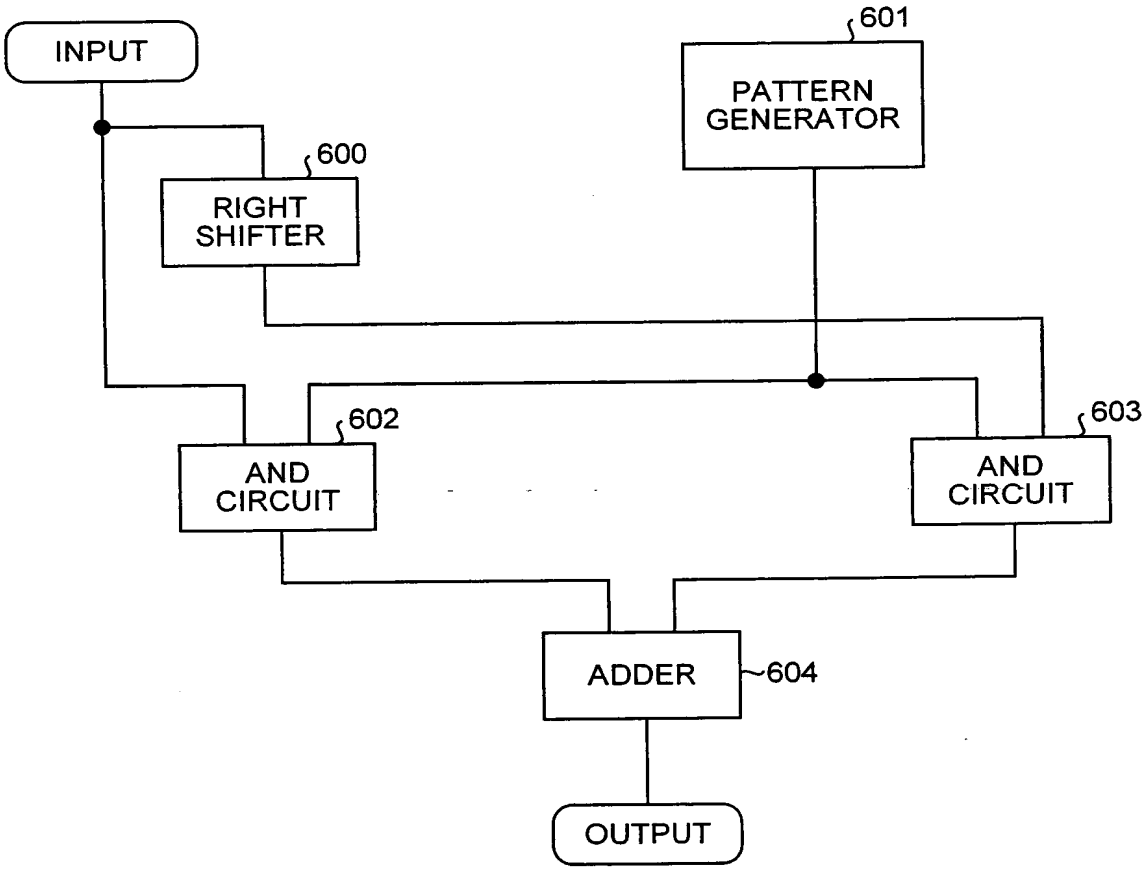

INPUT
601
PATTERN GENERATOR
600
RIGHT SHIFTER
602
AND CIRCUIT
603
AND CIRCUIT
ADDER
604
OUTPUT

FIG.7

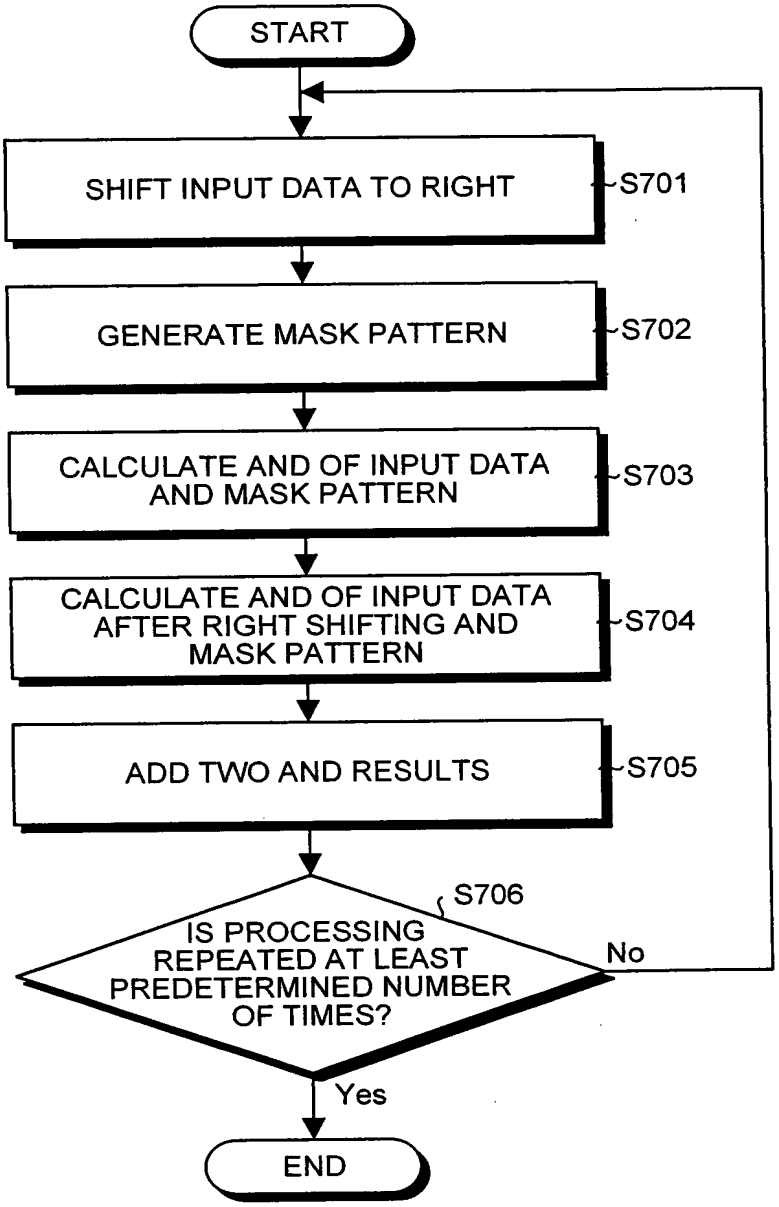

START
SHIFT INPUT DATA TO RIGHT
S701
GENERATE MASK PATTERN
S702
CALCULATE AND OF INPUT DATA AND MASK PATTERN
S703
CALCULATE AND OF INPUT DATA AFTER RIGHT SHIFTING AND MASK PATTERN
S704
ADD TWO AND RESULTS
S705
S706
IS PROCESSING REPEATED AT LEAST PREDETERMINED NUMBER OF TIMES?
No
Yes
END

FIG.8

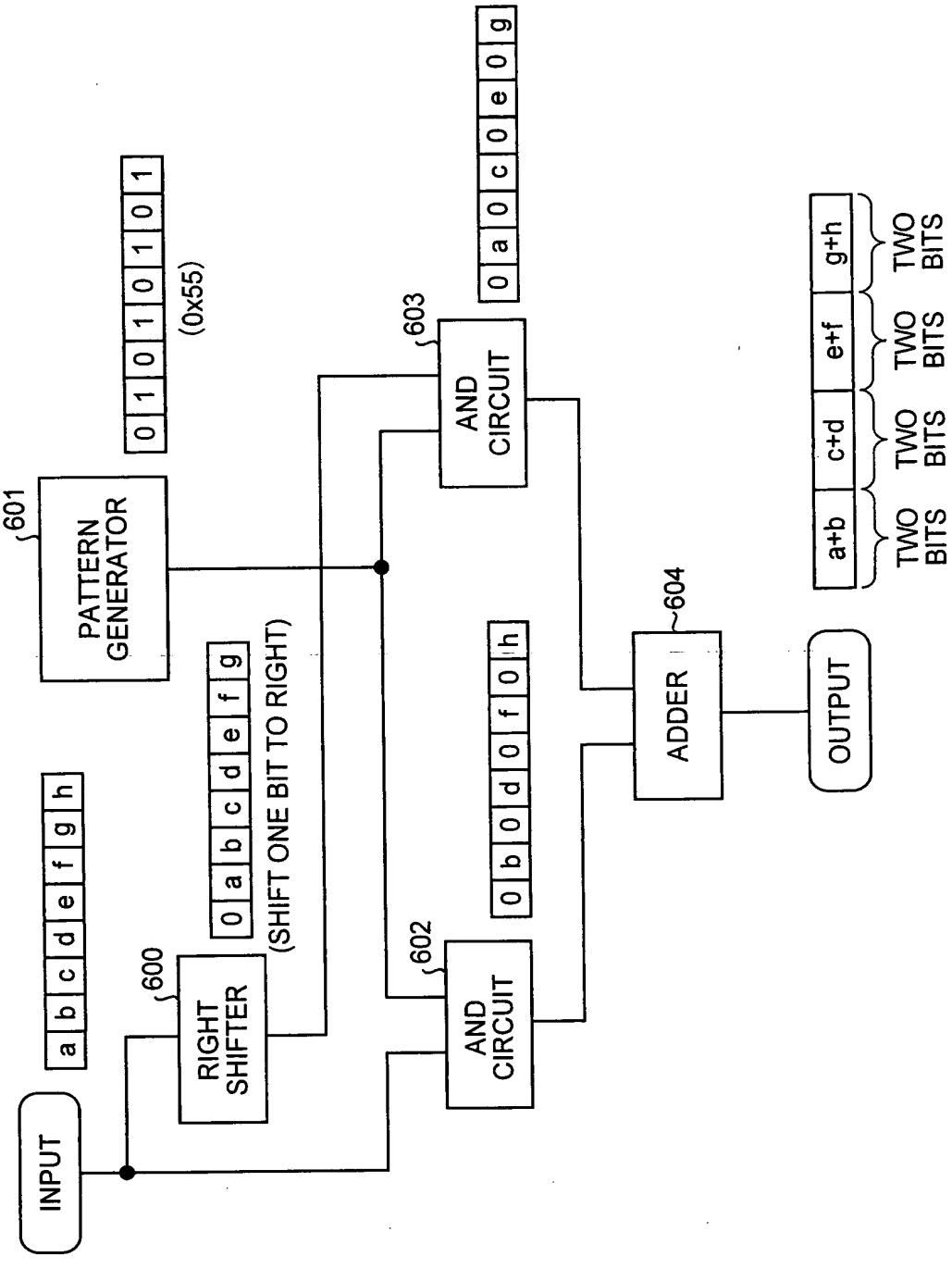

INPUT
a b c d e f g h
RIGHT SHIFTER
600
0 a b c d e f g
(SHIFT ONE BIT TO RIGHT)
PATTERN GENERATOR
601
0 1 0 1 0 1 0 1
(0x55)
AND CIRCUIT
602
0 b 0 d 0 f 0 h
AND CIRCUIT
603
0 a 0 c 0 e 0 g
ADDER
604
OUTPUT
a+b
c+d
e+f
g+h
TWO BITS
TWO BITS
TWO BITS
TWO BITS

FIG.9

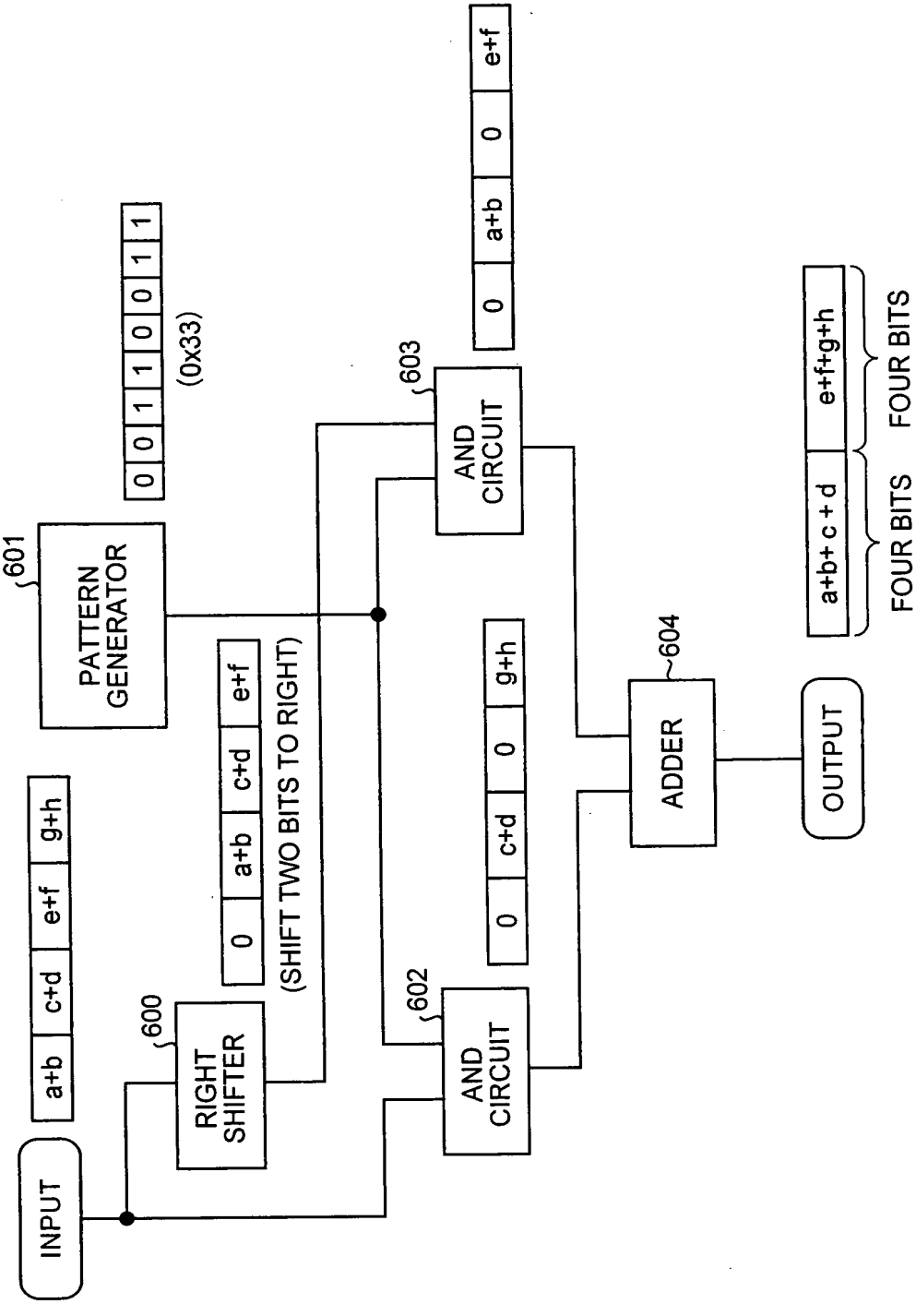

INPUT
a+b
c+d
e+f
g+h
600
RIGHT SHIFTER
0
a+b
c+d
e+f
(SHIFT TWO BITS TO RIGHT)
601
PATTERN GENERATOR
0 0 1 1 0 0 1 1
(0x33)
602
AND CIRCUIT
0
c+d
0
g+h
603
AND CIRCUIT
0
a+b
0
e+f
604
ADDER
OUTPUT
a+b+ c + d
e+f+g+h
FOUR BITS
FOUR BITS

FIG.10

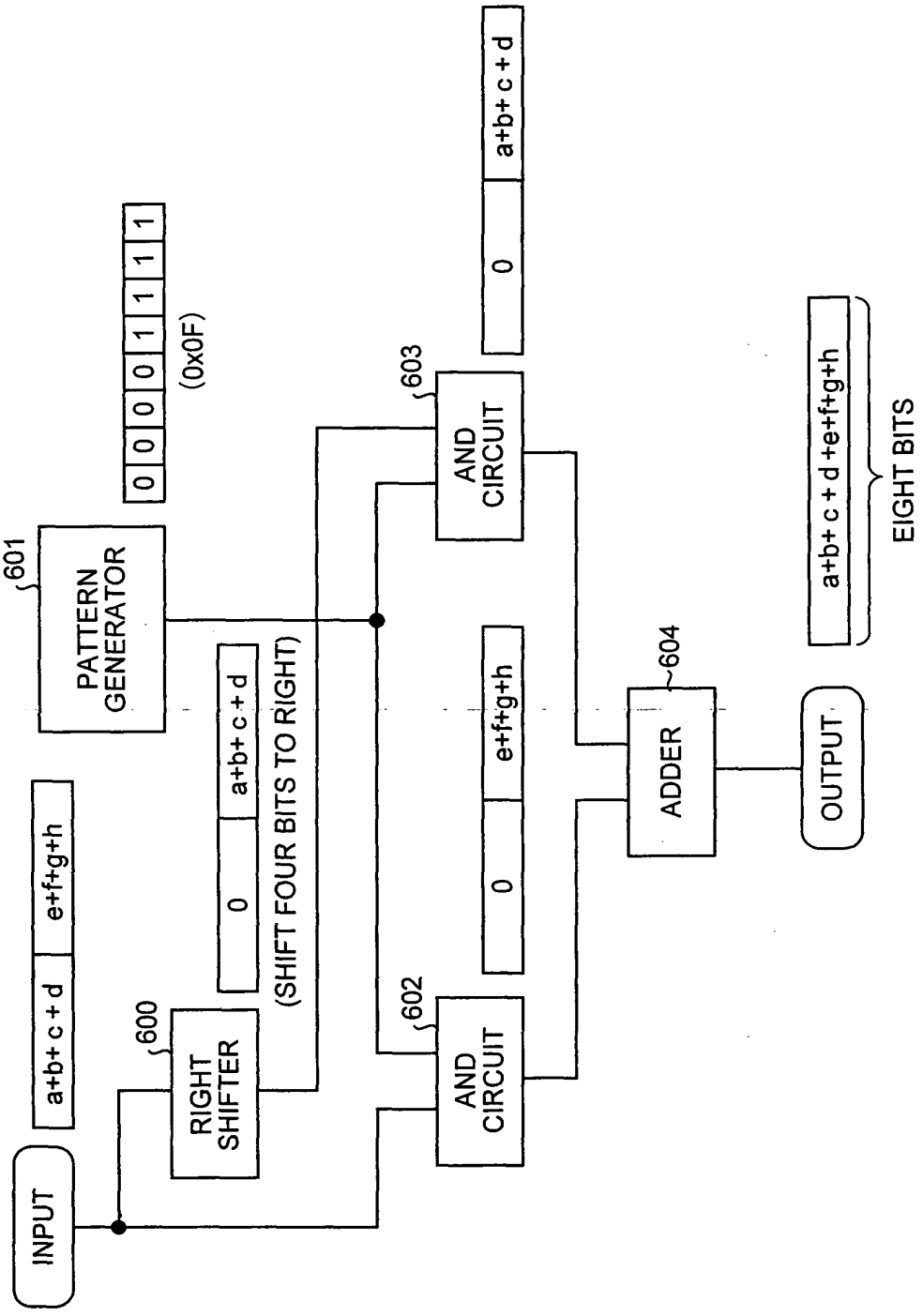

INPUT
a+b+ c + d
e+f+g+h
600
RIGHT SHIFTER
0
a+b+ c + d
(SHIFT FOUR BITS TO RIGHT)
601
PATTERN GENERATOR
0 0 0 0 1 1 1 1
(0x0F)
602
AND CIRCUIT
0
e+f+g+h
603
AND CIRCUIT
0
a+b+ c + d
604
ADDER
OUTPUT
a+b+ c + d +e+f+g+h
EIGHT BITS

FIG.11

		8 BITS	32 BITS
FIRST TIME	SHIFT QUANTITY	1	1
	MASK PATTERN	01010101(0x55)	01010101 01010101 01010101 01010101 (0x55555555)
SECOND TIME	SHIFT QUANTITY	2	2
	MASK PATTERN	00110011(0x33)	00110011 00110011 00110011 00110011 (0x33333333)
THIRD TIME	SHIFT QUANTITY	4	4
	MASK PATTERN	00001111(0x0F)	00001111 00001111 00001111 00001111 (0x0F0F0F0F)
FOURTH TIME	SHIFT QUANTITY		8
	MASK PATTERN		00000000 11111111 00000000 11111111 (0x00FF00FF)
FIFTH TIME	SHIFT QUANTITY		16
	MASK PATTERN		00000000 00000000 11111111 11111111 (0x0000FFFF)

FIG.12

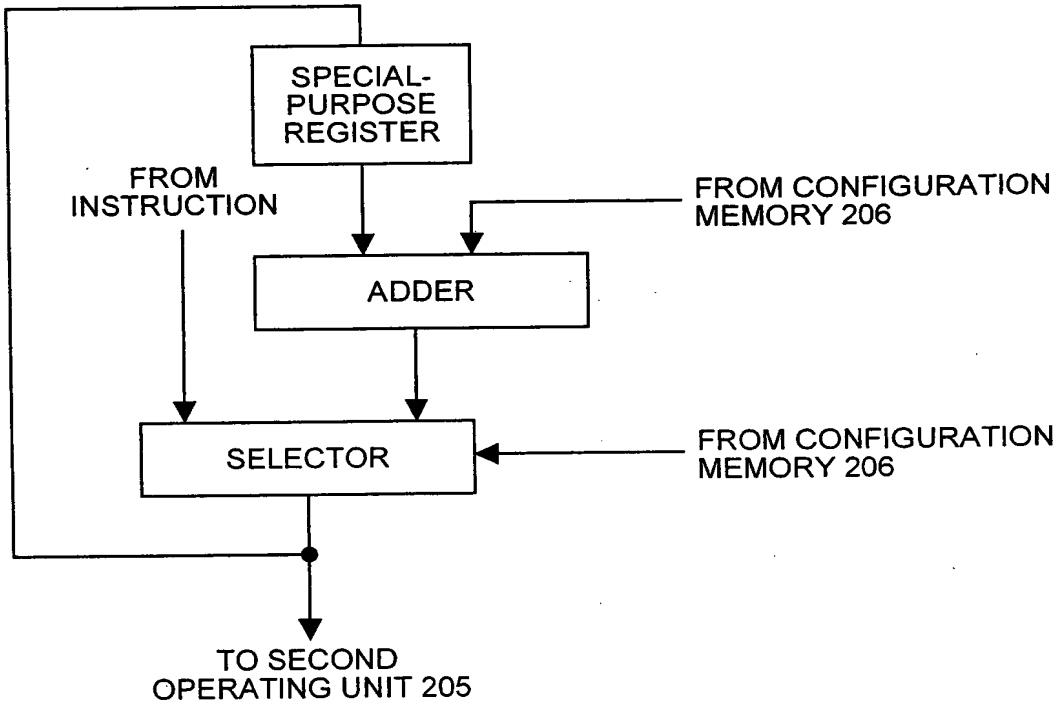

SPECIAL-
PURPOSE
REGISTER
FROM
INSTRUCTION
FROM CONFIGURATION
MEMORY 206
ADDER
SELECTOR
FROM CONFIGURATION
MEMORY 206
TO SECOND
OPERATING UNIT 205

FIG.13

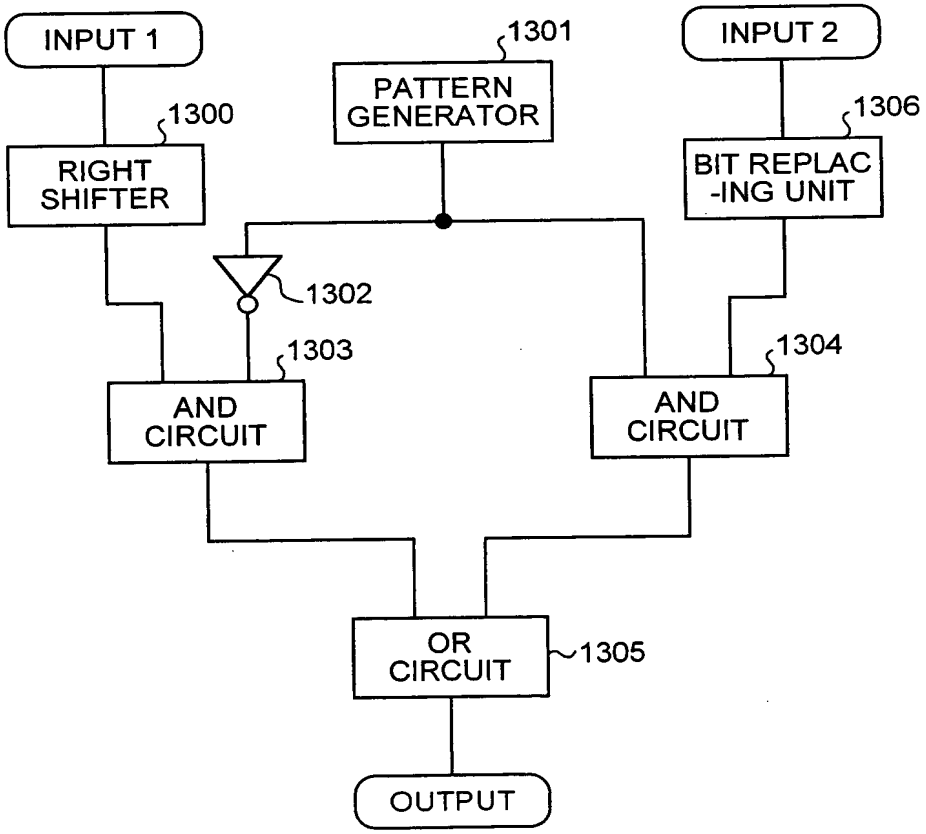

INPUT 1
1301
INPUT 2
1300
PATTERN
GENERATOR
1306
RIGHT
SHIFTER
BIT REPLAC
-ING UNIT
1302
1303
1304
AND
CIRCUIT
AND
CIRCUIT
OR
CIRCUIT
1305
OUTPUT

FIG.14

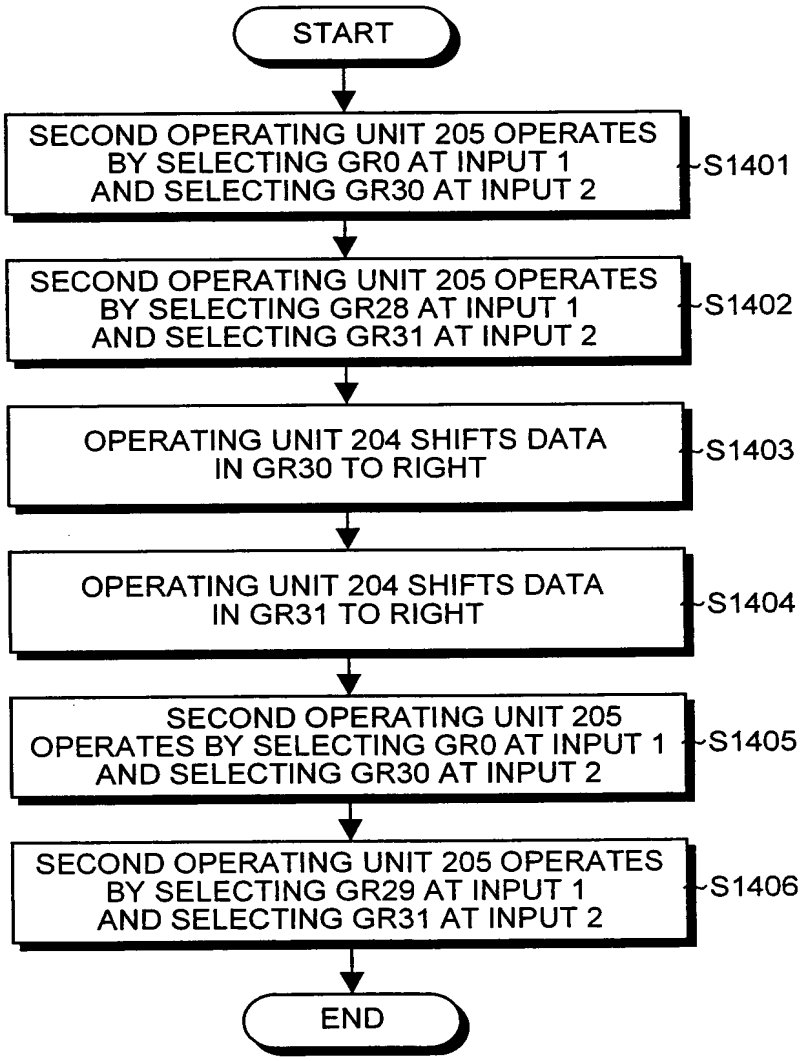

START
SECOND OPERATING UNIT 205 OPERATES BY SELECTING GR0 AT INPUT 1 AND SELECTING GR30 AT INPUT 2
S1401
SECOND OPERATING UNIT 205 OPERATES BY SELECTING GR28 AT INPUT 1 AND SELECTING GR31 AT INPUT 2
S1402
OPERATING UNIT 204 SHIFTS DATA IN GR30 TO RIGHT
S1403
OPERATING UNIT 204 SHIFTS DATA IN GR31 TO RIGHT
S1404
SECOND OPERATING UNIT 205 OPERATES BY SELECTING GR0 AT INPUT 1 AND SELECTING GR30 AT INPUT 2
S1405
SECOND OPERATING UNIT 205 OPERATES BY SELECTING GR29 AT INPUT 1 AND SELECTING GR31 AT INPUT 2
S1406
END

FIG.15

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

FIG.16

58	50	42	34	26	18	10	2
60	52	44	36	28	20	12	4
62	54	46	38	30	22	14	6
64	56	48	40	32	24	16	8
57	49	41	33	25	17	9	1
59	51	43	35	27	19	11	3
61	53	45	37	29	21	13	5
63	55	47	39	31	23	15	7

FIG.17A

BEFORE REPLACING BITS

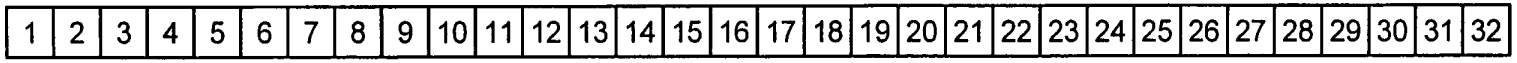


FIG.17B

AFTER REPLACING BITS

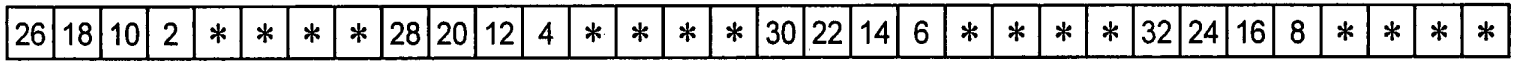


FIG.18

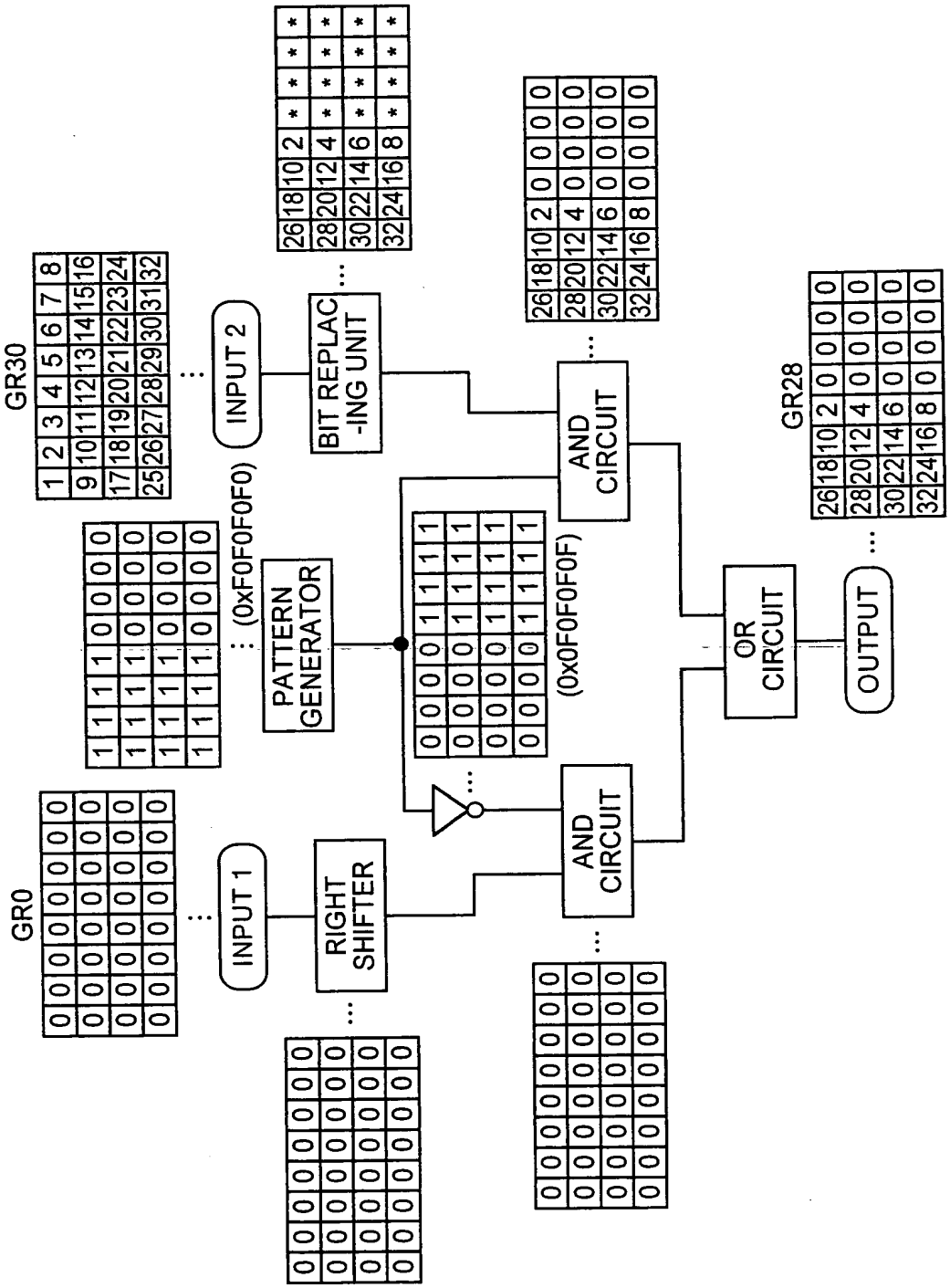

GR0
INPUT 1
RIGHT SHIFTER
GR30
INPUT 2
BIT REPLAC -ING UNIT
PATTERN GENERATOR
(0xF0F0F0F0)
(0x0F0F0F0F)
AND CIRCUIT
AND CIRCUIT
OR CIRCUIT
OUTPUT
GR28

FIG.19

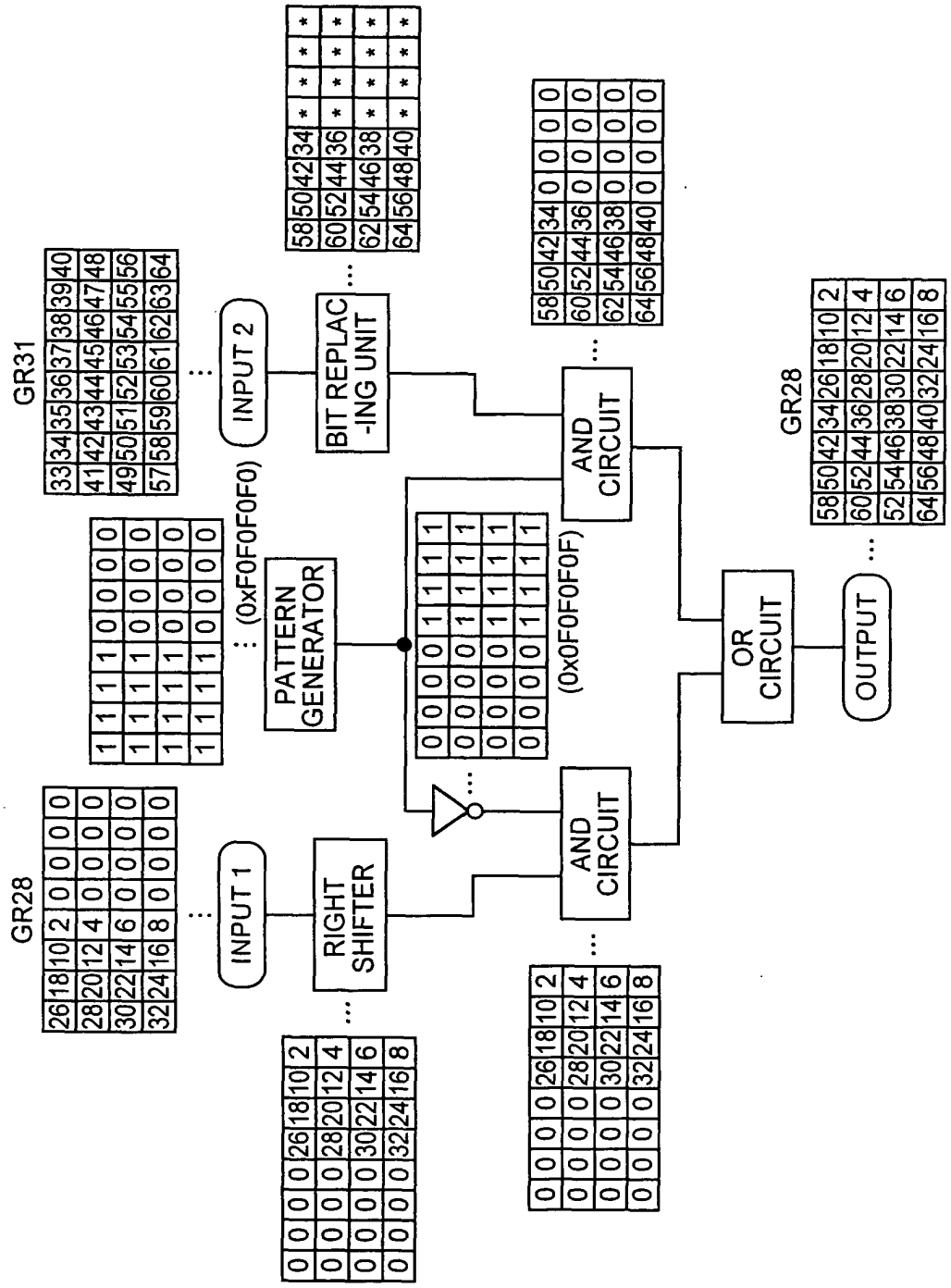

GR28
GR31
INPUT 1
INPUT 2
RIGHT SHIFTER
PATTERN GENERATOR
(0xF0F0F0F0)
BIT REPLAC -ING UNIT
AND CIRCUIT
AND CIRCUIT
(0x0F0F0F0F)
OR CIRCUIT
OUTPUT
GR28

FIG.20

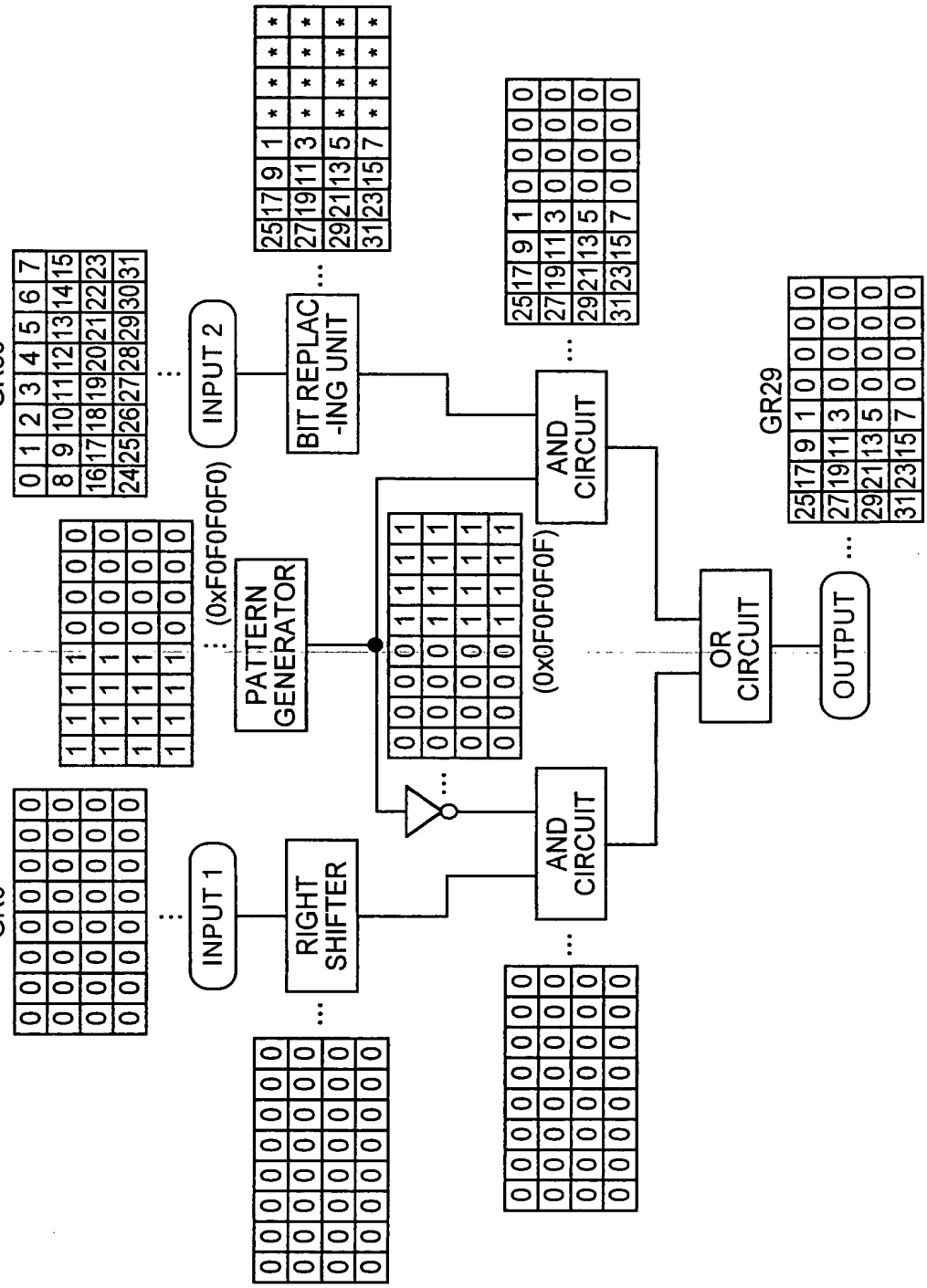

GR0
INPUT 1
RIGHT SHIFTER
GR30
INPUT 2
BIT REPLAC -ING UNIT
PATTERN GENERATOR
(0xF0F0F0F0)
AND CIRCUIT
AND CIRCUIT
(0x0F0F0F0F)
OR CIRCUIT
OUTPUT
GR29

FIG.21

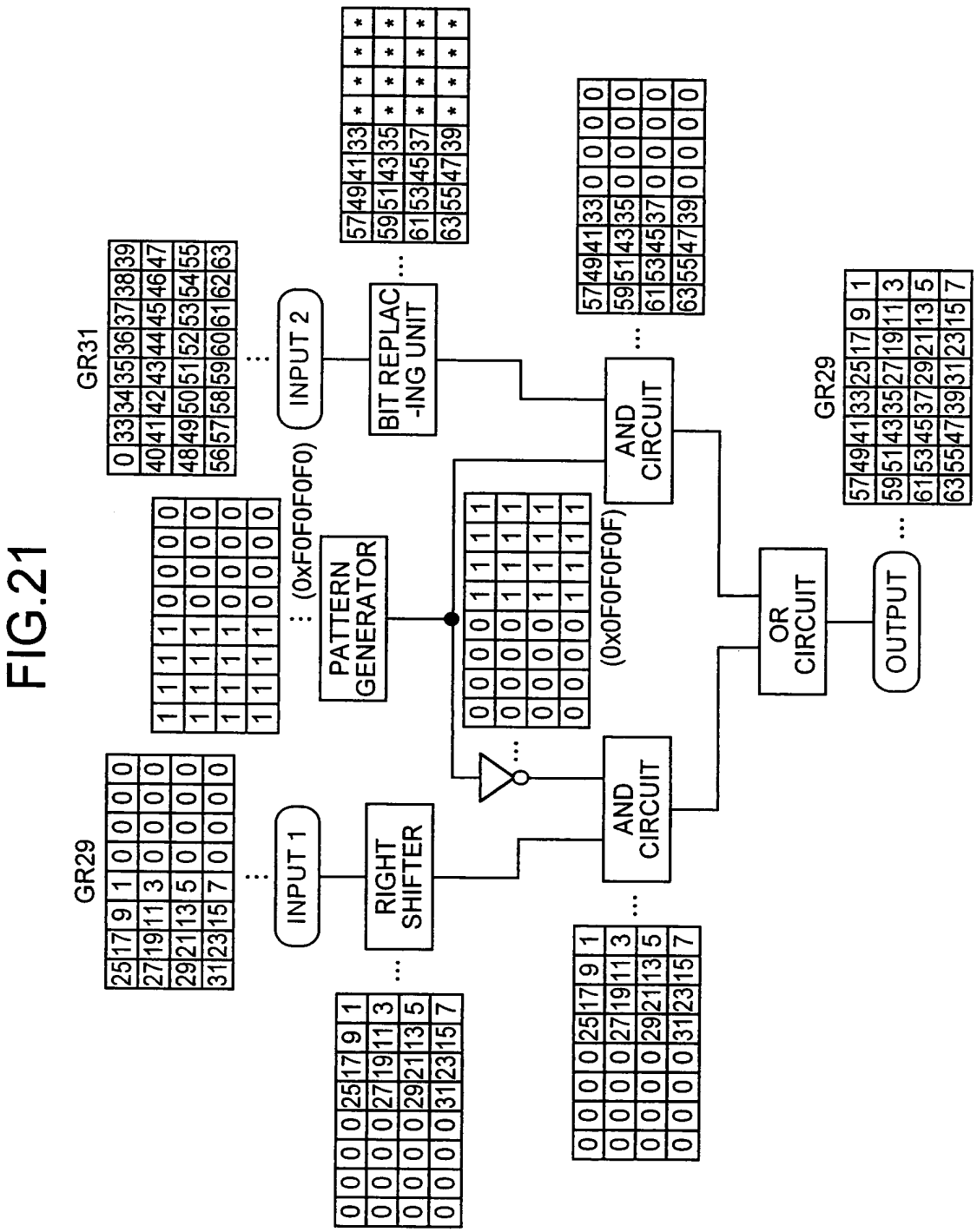

GR29
GR31
INPUT 1
INPUT 2
RIGHT SHIFTER
PATTERN GENERATOR
(0xF0F0F0F0)
BIT REPLAC -ING UNIT
AND CIRCUIT
AND CIRCUIT
(0x0F0F0F0F)
OR CIRCUIT
OUTPUT
GR29

FIG.22

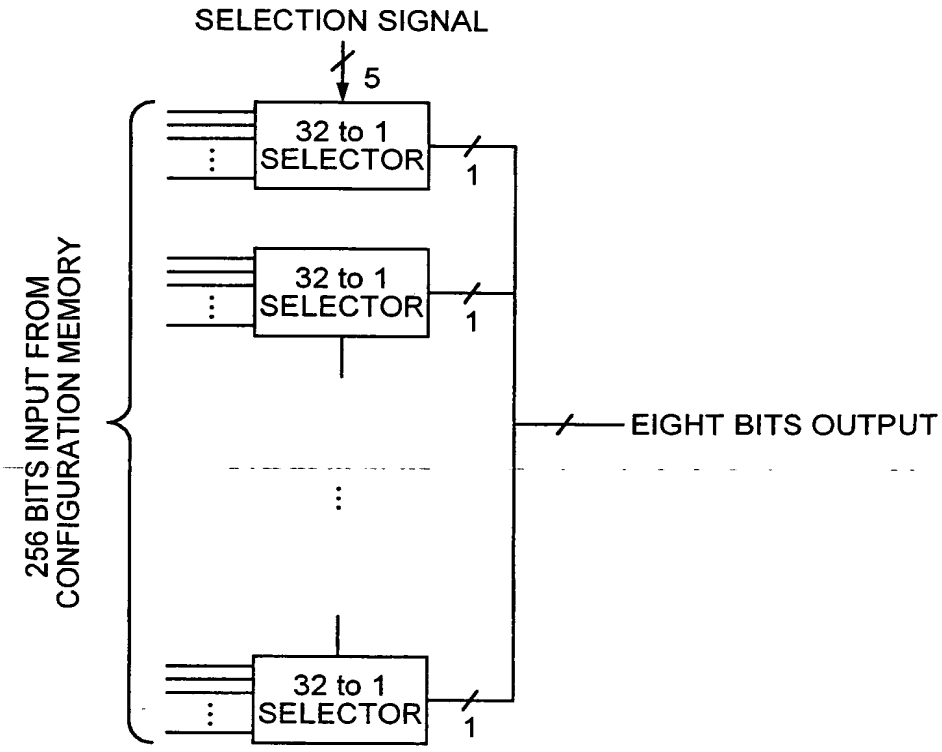

SELECTION SIGNAL
5
32 to 1 SELECTOR
1
32 to 1 SELECTOR
1
32 to 1 SELECTOR
1
256 BITS INPUT FROM CONFIGURATION MEMORY
EIGHT BITS OUTPUT

FIG.23

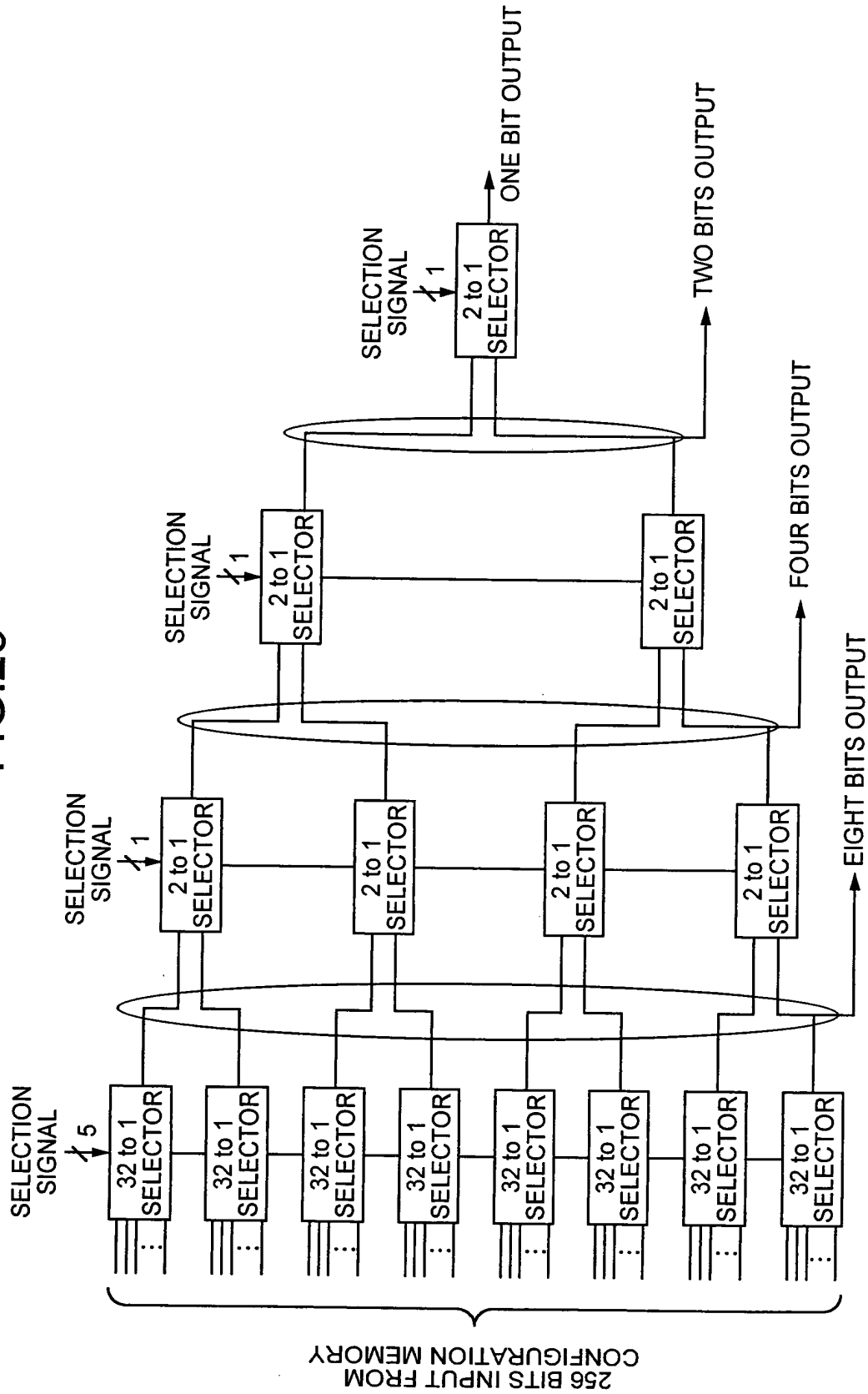
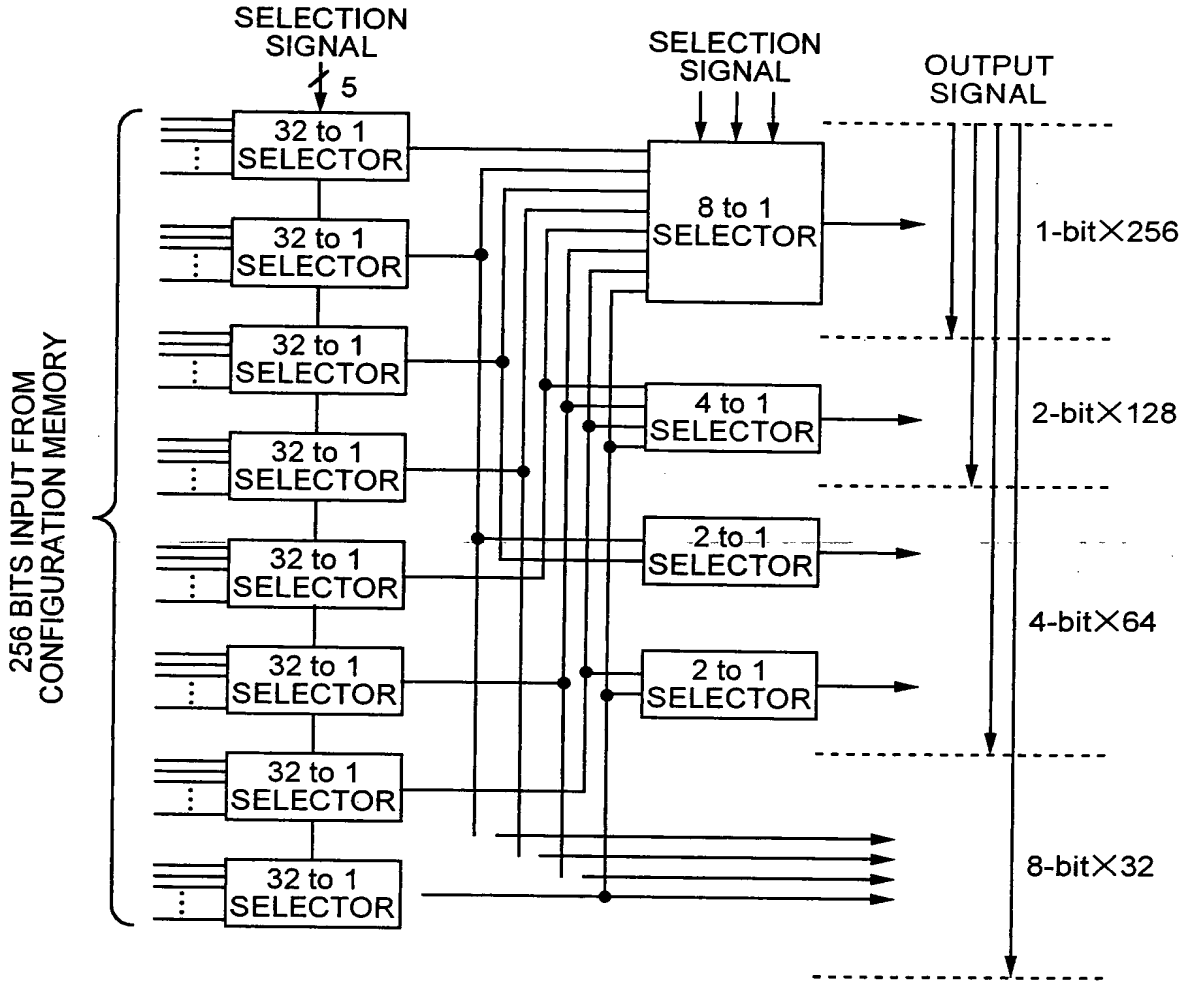

256 BITS INPUT FROM CONFIGURATION MEMORY
SELECTION SIGNAL 5
32 to 1 SELECTOR
SELECTION SIGNAL 1
2 to 1 SELECTOR
EIGHT BITS OUTPUT
SELECTION SIGNAL 1
2 to 1 SELECTOR
FOUR BITS OUTPUT
SELECTION SIGNAL 1
2 to 1 SELECTOR
TWO BITS OUTPUT
SELECTION SIGNAL 1
2 to 1 SELECTOR
ONE BIT OUTPUT

FIG.24


SELECTION SIGNAL
5
SELECTION SIGNAL
OUTPUT SIGNAL
256 BITS INPUT FROM CONFIGURATION MEMORY
32 to 1 SELECTOR
32 to 1 SELECTOR
32 to 1 SELECTOR
32 to 1 SELECTOR
32 to 1 SELECTOR
32 to 1 SELECTOR
32 to 1 SELECTOR
32 to 1 SELECTOR
8 to 1 SELECTOR
4 to 1 SELECTOR
2 to 1 SELECTOR
2 to 1 SELECTOR
1-bit×256
2-bit×128
4-bit×64
8-bit×32